UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/667,825	09/22/2003	Giuseppe Pedretti	8245.060	1009

30589 7590 01/26/2007
DUNLAP, CODDING & ROGERS P.C.
PO BOX 16370
OKLAHOMA CITY, OK 73113

EXAMINER	
PHAN, THIEM D	
ART UNIT	**PAPER NUMBER**
3729	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/26/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/667,825	PEDRETTI ET AL.	
	Examiner	Art Unit	
	Tim Phan	3729	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12/11/07*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6-12 and 25-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-12 and 25-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicants' submission filed on 12/11/06 has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 2, 6-8, 25, 26 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Patel et al (US 6,623,651 B2) in view of Gilleo et al (US 5,637,176)9.

With regard to claims 1 and 25, Patel et al teach a method for making circuit board,

comprising:

- forming a conductor core (Fig. 1B, 20) containing a thin base (Fig. 1B, 18) of electrically conductive material and areas of thick conductive material (Fig. 1B, 15), the thick conductive material in a predetermined pattern (Fig. 1B, 15) of conductor traces extending laterally on the thin base;
- bonding the conductor core to a sublayer (Fig. 1C, 22) of electrically insulating material to create a flat laminate (Fig. 1C, 10), wherein the areas of thick conductive material (Fig. 1C, 15) are positioned adjacent to the sublayer (Fig. 1C, 22); except for being covered by the sublayer, which is well known in the art;
- forming predetermined printed circuits (Fig. 1F, 10) having both thick conductor traces formed from the thick conductive material (Fig. 1F, see below) and fine resolution traces from the thin base (Fig. 1F, see below) by/and removing conductive material (Fig. 1F, elements 44d-44f) from the flat laminate that does not comprise said predetermined printed circuits (Fig. 1E, 40) to form the predetermined printed circuits (Fig. 1G, 48).

Gilleo et al teach a method of producing adhesive materials (Fig. 8A) for electronic components with printed circuit board with a step of covering or doctor-blade covering conductive columns or tracks of dielectric paste (Fig. 4C) to be dried, hardened and polished or grinded off.

It would be obvious to one of ordinary skill in the art at the time the invention was made to combine the two teachings by having conductive layer set with dielectric material, as taught by Gilleo et al and not its general structure, to the method for making circuit board as taught by

Patel et al with the conductive material set next to the dielectric one, as a simple process to lay the dielectric material on a conductive one.

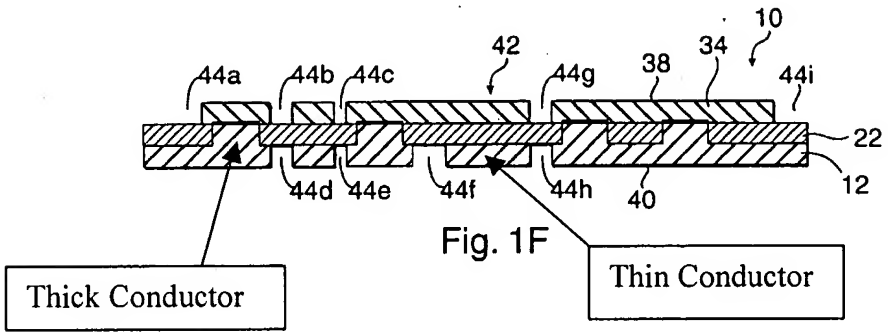


Fig. 1F

With regard to claims 2 and 26, Patel et al teach that the conductor core (Fig. 1B) and predetermined printed circuits (Fig. 1G, 48) comprise copper.

With regard to claim 6, Gilleo et al teach that the bonding is performed at sufficient temperature and time to complete cure the resin (Fig. 4D).

With regard to claims 7 and 31, Patel et al teach that the removing of conductive material is accomplished through chemical etching or etchant material by a conventional etching process (Fig. 1F, 44d-44h; col. 4, line 30; col. 3, line 54).

With regard to claim 8, Patel et al teach a method for making circuit board, including the etching process (Col. 4, line 30) of the conductive areas to form predetermined areas (Fig. 1G, 48) of the PCB, which reads on Applicants' claimed invention except for describing a solder mask coating.

It would be obvious to one of ordinary skill in the art at the time the invention was made to apply a solder mask coating in order to accomplish an etching process.

3. Claims 3, 4, 9-12, 27-30 and 32-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Patel et al in view of Gilleo et al and futher view of Bokisa (US 5,928,790).

With regard to claims 3 and 27, Patel et al in view of Gilleo et al teach a method for making circuit board, including the formation of conductor core with thick and thin conductive base areas, which reads on Applicants' claimed invention except for depositing a conductive base area upon another one in order to thicken it.

Bokisa teaches a process of making multilayer circuit boards with a step of depositing a conductive layer on another circuitry layer (Col. 5, lines 61 ff.) for thickness and accuracy.

It would be obvious to one of ordinary skill in the art at the time the invention was made to combine the three teachings, by applying the deposition process as taught by Bokisa to thicken the conductor base area of Patel et al, for better accuracy.

With regard to claims 4 and 28, Patel et al teach a method for making circuit board, including the formation of a sublayer (Fig. 1C, 22) of electrically insulating material, which reads on Applicants' claimed invention except for the sublayer of electrically insulating material that comprises sheets of glass fiber reinforced with resin that is dried but not cured or prepreg, which is well known in this art.

Bokisa teaches a process of making multilayer circuit boards with a partially cured prepreg as non-conductive layer (Col. 1, lines 13 ff.) in a multilayer board, which is old art.

It would be obvious to apply a prepreg as non-conductive layer in a multilayer circuit in order to isolate the circuitry.

With regard to claims 9-12 and 32-35, Patel et al and Bokisa teach a process of making multilayer circuit board, including the conductor circuitry thickness about four one-thousandths of an inch (Patel et al; col. 3, line 48) or 2 to 4 microns (Bokisa; col. 5, lines 32 ff.) except for assigning multiple different thickness ranges for the conductor traces.

It is mere matter of design choice to assign different thickness ranges for the conductor traces and it is held that the claimed temperature ranges are not so critical as to be novel or unobvious over the thickness range recited in the Patel et al and Bokisa's arts.

With regard to claims 29 and 30, Bokisa teaches the timely heating and pressure exerted on the prepreg for bonding (Col. 1, lines 14 ff.) to the conductor core, which is also old in this art.

Response to Arguments

4. Applicants' arguments filed 12/11/06 have been fully considered but they are not persuasive for the following reasons:

Applicants assets that the prior art Patel et al does not teach thick and thin conductors for

power circuits and fine resolution conductors rather than bumps, vias or protuberances (Remarks, pages 9-11). First, in response to applicants' argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., single layer, fine resolution conductor, nubs, bumps, protuberances, ...) are not recited in the rejected claims. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Second, it appears that applicants fail to recognize the scope of the claims when judged in view of the Patel et al, especially with respect to the thick and thin conductive base material (See Fig. 1F above). (Cf. MPEP 2111 and *In re Geuns*, 26 USPQ 2nd 1057 (Fed. Cir. 1993)).

In response to applicant's arguments that there is no covering of the thick layer by dielectric material (Pages 12-14), they are moot in view of the new and current grounds of rejection.

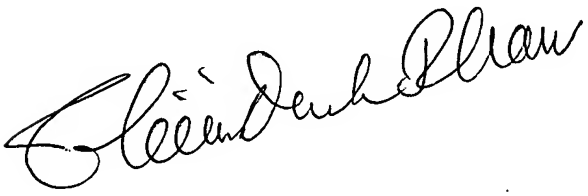
Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicants' disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tim Phan whose telephone number is 571-272-4568. The examiner can normally be reached on M & Tu, 6AM - 2PM, and W & Th, 9AM – 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Peter Vo can be reached on 571-272-4690. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Tim Phan
Examiner
Art Unit 3729

tp
January 22, 2007